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Comparative Study of Symmetric and Asymmetric Oxide Double Gate Junction less FET

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***Abstract* – We carry out the performance of symmetric oxide (HfO2+HfO2) and asymmetric oxide (SiO2+HfO2) n-type junction less field-effect transistor (JLFET) based on two- dimensional Poisson equation. This study is accomplished by simulating a symmetric and asymmetric double gate JLFET on Sentaurus, Technology Computer Aided Design (TCAD) simulator for Silicon (Si) material at room temperature and varying temperature in between 300-360 K. Based on device simulation we find that the asymmetric oxide shows preferable performance in terms of ON-state current (ION), subthreshold swing (SS), the ION/IOFF ratios (~10^7) and the equivalent oxide thickness (EOT) compared to symmetric devices and also asymmetric oxide technology enhances the performance and reduces the power consumptions.**

Keywords-EOT; Symmetric; TCAD; SS.

I. INTRODUCTION

As the scaling of semiconductor device CMOS influences its breaking points the value of short channel effects (SCEs) increases actively as a result of weak control of gate over the channel. To overcome this obstacle several new type of semiconductor devices proposed such as multi-gate MOSFETs, FinFETs, TFETs etc. [1], In all these above devices channel is strongly controlled by Gate. In spite of, as the gate length decreases below 10-5nm excessive doping concentration gradient needed in source and drain junctions, that is a big demand and difficulty in device design both in fabrication and budgets [2-3]. To solve the issue a new semiconductor device proposed that works without the formation of junctions in source-channel and drain-channel areas.

A junction less FET is close to a gated resistor with similar doping in source to drain, hence there is no issues related to doping also, there is no metallic junctions in between source to channel and channel to drain interface. The fabrication process and production cost of JLFET is less compared to Metal oxide FET [4], Therefore, JLFETs seems to be a encouraging substitute to the standard MOSFETs.

As contrast to the standard gated MOSFETs, JLFETs have lots of superiority such as the processing is out of diffusion issues, no channel conductivities on account of highly doped Si, lower value of gate capacitances and also the subthreshold slope values are lower. Remarkably it became most interesting semiconductor device for scaling, low process flow and thermal budgets. Basically, JL FETs is a resistor with constantly steadily doped all around the device regions, source, channel and drain [5-6].

The vacancy of doping concentration gradients drives out diffusion process. Due to lack of Diffusion the cost of annealing is lowered and also the device with lower channel length is fabricated [7-8]. In this work we try to investigate the impact of temperature, High-k dielectric materials and Gate work function on the double gate junction less FET in case of symmetric and asymmetric type-high k oxide used with the same oxide thickness on the double gate JLFET device [9].

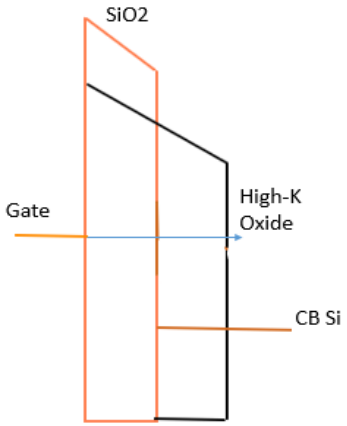

Figure. 1. Graphic of Direct tunneling through SiO2 and difficult tunneling through High-k Oxide (HfO2).

II. DEVICE SIMULATION SETUP

Device structure of the double Gate symmetric and asymmetric oxide junction less FET are shown in Figure2. The prime difference between the two device structures is that in primary structure used a combination of SiO_2 and HfO_2 as high-k dielectric whereas in latter only HfO_2 used. It was found that HfO_2 (K =25, Gap(eV)=5.8, CB offset (eV)=1.4) [10] used device have better tunneling probability and in the presence of HfO_2 as a high k material the device have also lower leakage current. For Si devices mostly HfO_2-based high k oxide is used due to lower thermal stabilities and also reasonable permittivity's. The specifications used in the JLFET device simulation are shown in Table 1. To assure the enough gate control the value of EOT and silicon body thickness are chosen small. The source, channel and drain sections are doped uniformly with active phosphorus with a doping value of 10^{20} cm^{-3}.

TABLE I. SPECIFICATIONS USED IN TCAD SETUP FOR JLFE

Parameters	Value
Gate length	30nm
Supply voltage	1V
Source drain channel doping	10^{20} cm^{-3}
Gate metal work fun	5.2ev
Effective oxide thickness	1nm
Channel thickness	20 nm

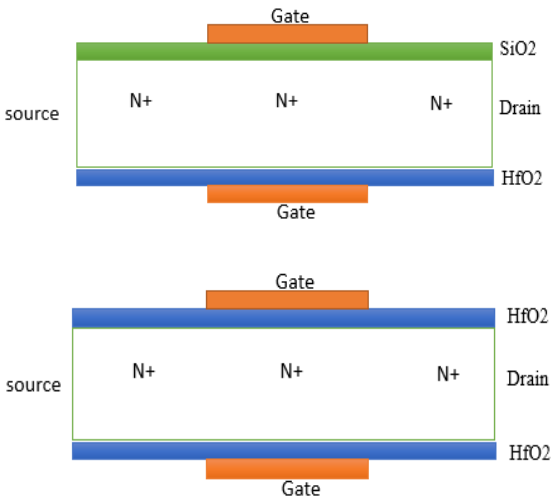

Figure. 2. Schematic device structures of symmetric and asymmetric oxide JLFET with an EOT value of 1 nm and Lch = 20 nm.

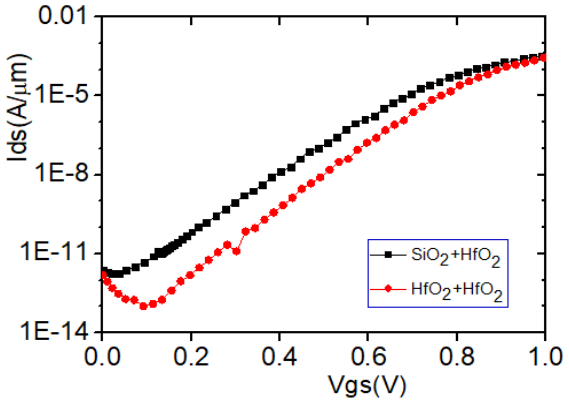

Figure.3. Measured output characteristics (I_{ds}-V_{gs}) of symmetric and asymmetric oxide JLFET (V_{ds}=1V)

III. SIMULATION RESULT AND DISCUSSION

The JLFET device Simulations were driven out through Sentaurus TCAD simulation software. High Field Saturation mobility model was considered for doping dependent mobility. Shockley-Read Hall (SRH), Band to Band Non local path model and Fermi-Dirac statistics were also implemented. Bandgap narrowing (BGN) model included in the device simulation.

The output characteristics of both asymmetric oxide SiO_2/HfO_2 and symmetric oxide HfO_2/HfO_2 junction less device with channel length 20 nm is plotted in Figure 3, it can be clearly seen that the ON current and subthreshold swing of simulated device is more in case of asymmetric oxide SiO_2 and HfO_2 operated device and also an I_{ON} /I_{OFF} of 10^7 is achieved at V_g=1V. This result is comparatively large compared to result obtained in [11]. Although as the case may be noted that the main purpose of this work is to demonstrate the relative performance effect of the combination of high-k oxide on the electrical aspects of the junction less FET.

A. Temperature Characteristics

To study the carrier transport mechanisms in symmetric and asymmetric oxide junction less FET temperature measurements were performed, that display that in case of JLFETs the threshold voltage variation is more compared to standard MOSFETs, also there is no "zero temperature coefficient" (ZTC) point is noticeable in junction less device at lower temperature range.

To extract the temperature effects of high values and effects of temperature on electric fields distribution, electric field craving on mobility, the model used in the equivalent transfer characteristics are shown in Figure 4. within the temperature range of 300-360 K, the value of off currents decreases with increase of temperature this can be as a result of increment at high temperature [12], the value of intrinsic carrier concentration.

The value of on current in case of Asymmetric high-K oxide used device lowered with T increased

for the reason that the decrement of mobility by serious phonon scattering at above the room temperature [13].

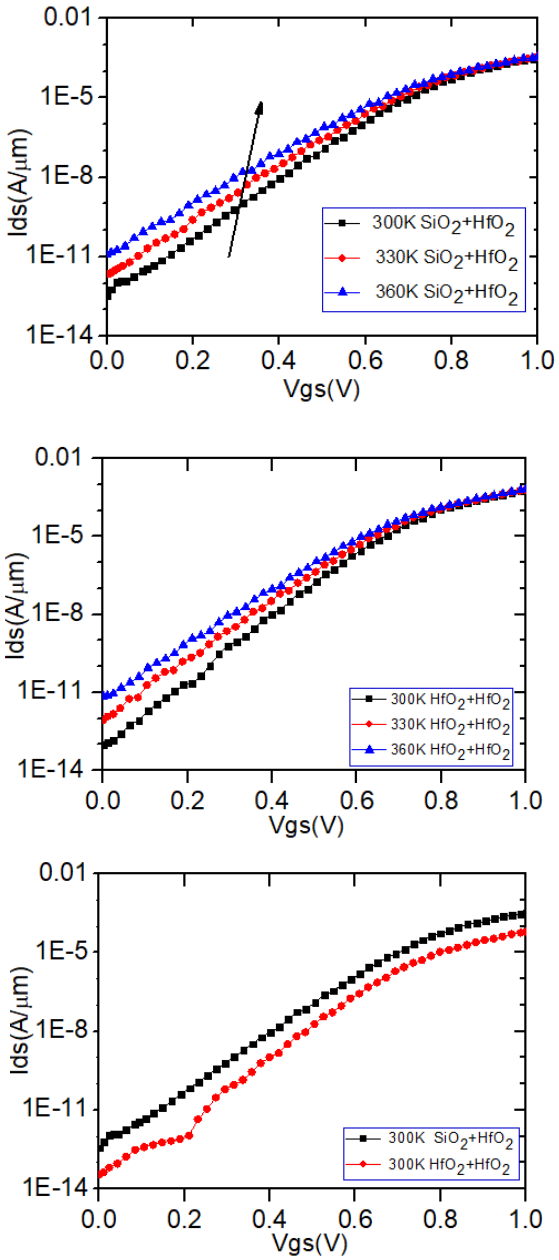

Figure 4. Schematic device structures of symmetric and asymmetric oxide JLFET with an EOT value of 1 nm and Lch = 40 nm and temperature varies from 300-360 (K)

B. Work Function Characteristics

To turn on the JLFET threshold voltage is chosen precisely which is the work function of channel and gate material used, the value of inequalities between work function used in channel and material used in gate part of device should be small so that the semiconductor device has a low threshold voltage and device turn on in a fast way. we use TCAD simulation to address the work function variation on the device output current. The metal gate work function changes between 4.8(eV) to 5.2 (eV), it influences electrostatic integrity of devices as shown in the Figure 4.

The Short Channel Effect for JLFET is dependent upon the work function variation [14] principal to make a remark on I_{ON}/I_{OFF}, and Subthreshold Slope variation more in case of asymmetric oxide junction less FET.

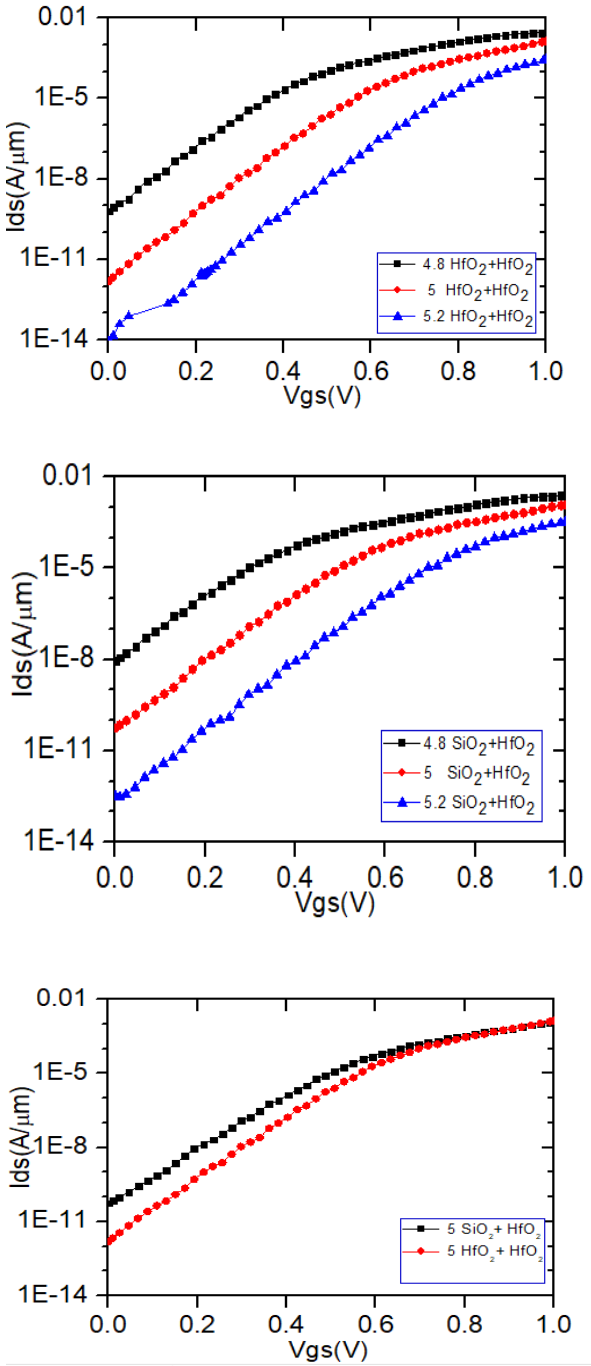

Figure 5. Schematic device structures of symmetric and asymmetric oxide JLFET with an EOT value of 1 nm and Lch = 40 nm work function varies from 4.8-5.2 (eV).

C. Impact of EOT

The subthreshold swing depends on gate materials and the gate oxide thickness for various gate oxide materials, As the dielectric constant increases, the subthreshold swing decreases. The changing rate of the subthreshold swing decreases with the changing rate of the gate oxide film thickness as the dielectric

constant increases. Also, as the dielectric constant increases, the subthreshold swing sharply decreases.

Figure 5 shows the output characteristics of simulated Symmetric and Asymmetric oxide junction less FET, and the various device output characteristics is figure out by find out the carrier continuity and Poisson equations self-consistently with Fermi statistics at three different EOT values of 1, 2, 3 nm. Therefore, the on/off current ratio will increase according to increment of the dielectric constant and the Junction less FET doing will be improved

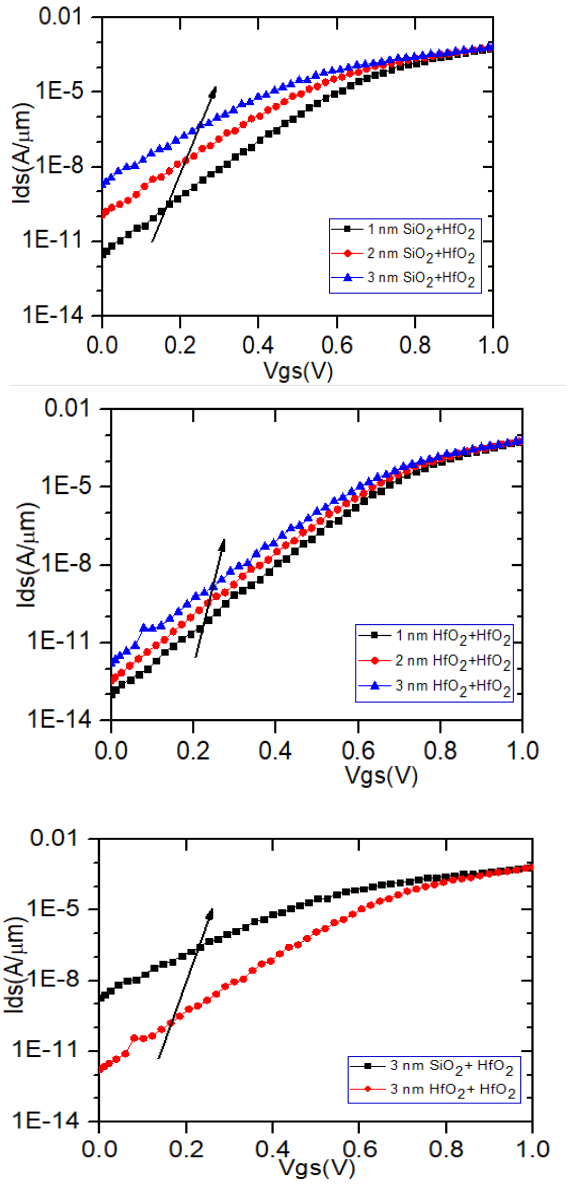

Figure 6. Schematic device structures of symmetric and asymmetric oxide JLFET with an EOT value of 1-3 nm and L_{ch} = 40 nm.

CONCLUSION

In short, the output characteristics of symmetric and asymmetric JLFET studied in temperature range 300-360K.Successfully authenticated combination of SiO_2 and HfO_2 Oxide to N-type junction less FET by Sentaurus device simulator and a comparative study was done, SS decreases with increase of dielectric constant also the trans conductance to I_d ratio is high for high dielectric constant materials. The asymmetric oxide device shows higher I_{ON}, which indicated higher switching speed and suppressed the SCE.

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